

CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:
5 forming a ferroelectric capacitor in a capacitor level above a semiconductor body; and
forming a low silicon-hydrogen SiN layer above the ferroelectric capacitor, the low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:
10 $\text{Si-H absorbance} / (\text{N-H absorbance} \times 1.4)$.

2. The method of claim 1, wherein forming the low silicon-hydrogen SiN layer comprises depositing a low silicon-hydrogen SiN material above the ferroelectric capacitor using a plasma enhanced chemical vapor deposition
15 process.

3. The method of claim 2, wherein depositing the low silicon-hydrogen SiN material comprises performing the plasma enhanced chemical vapor deposition process with an N₂ flow of about 10,000 sccm or more and an NH₃
20 flow of about 1,000 sccm or less.

4. The method of claim 3, wherein depositing the low silicon-hydrogen SiN material comprises performing the plasma enhanced chemical vapor deposition process with an N₂ flow of about 14,000 sccm or more.
25

5. The method of claim 4, wherein depositing the low silicon-hydrogen SiN material comprises performing the plasma enhanced chemical vapor deposition process with an NH₃ flow of about 750 sccm or less.

6. The method of claim 3, wherein depositing the low silicon-hydrogen SiN material comprises performing the plasma enhanced chemical vapor deposition process with an NH₃ flow of about 750 sccm or less.

5 7. The method of claim 2, wherein the low silicon-hydrogen SiN layer is one of an etch stop layer in the capacitor level, an etch stop layer in a metalization level above the capacitor level, and an etch stop layer in a protective oxide level above an uppermost metalization level.

10 8. The method of claim 7, further comprising forming a second low silicon-hydrogen SiN layer above a transistor in the semiconductor device, the second low silicon-hydrogen SiN layer being below the capacitor level, the second low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:

15
$$\text{Si-H absorbance} / (\text{N-H absorbance} \times 1.4).$$

9. The method of claim 8, wherein the second low silicon-hydrogen SiN layer is an etch stop layer in a poly-metal dielectric level.

20 10. The method of claim 2, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.04 or less.

11. The method of claim 2, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.03 or less.

25

12. The method of claim 1, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.04 or less.

13. The method of claim 12, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.03 or less.

30

TI-35995

14. The method of claim 1, wherein the low silicon-hydrogen SiN layer is one of an etch stop layer in the capacitor level, an etch stop layer in a metalization level above the capacitor level, and an etch stop layer in a protective oxide level above an uppermost metalization level.

15. The method of claim 14, wherein the low silicon-hydrogen SiN layer is an etch stop layer in the capacitor level.

16. The method of claim 14, wherein the low silicon-hydrogen SiN layer is an etch stop layer in a metalization level above the capacitor level.

17. The method of claim 14, wherein the low silicon-hydrogen SiN layer is an etch stop layer in a protective oxide level above an uppermost metalization level.

18. The method of claim 14, further comprising forming a second low silicon-hydrogen SiN layer above a transistor in the semiconductor device, the second low silicon-hydrogen SiN layer being below the capacitor level, the second low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:

$$\text{Si-H absorbance} / (\text{N-H absorbance} \times 1.4).$$

19. The method of claim 18, wherein the second low silicon-hydrogen SiN layer is an etch stop layer in a poly-metal dielectric level.

20. The method of claim 1, further comprising forming a second low silicon-hydrogen SiN layer above a transistor in the semiconductor device, the second low silicon-hydrogen SiN layer being below the capacitor level, the

second low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:

Si-H absorbance / (N-H absorbance x 1.4).

5 21. The method of claim 20, wherein the second low silicon-hydrogen SiN layer is an etch stop layer in a poly-metal dielectric level.

22. A method of fabricating a semiconductor device, comprising:
forming a ferroelectric capacitor in a capacitor level above a

10 semiconductor body; and

forming a low silicon-hydrogen SiN layer above a transistor in the semiconductor device, the low silicon-hydrogen SiN layer being below the capacitor level, the low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:

15 Si-H absorbance / (N-H absorbance x 1.4).

23. The method of claim 22, further comprising forming a second low silicon-hydrogen SiN layer above the ferroelectric capacitor, the second low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:

20

Si-H absorbance / (N-H absorbance x 1.4).

24. The method of claim 22, wherein forming the low silicon-hydrogen SiN layer comprises depositing a low silicon-hydrogen SiN material above the transistor using a plasma enhanced chemical vapor deposition process.

25

25. The method of claim 24, wherein depositing the low silicon-hydrogen SiN material comprises performing the plasma enhanced chemical vapor deposition process with an N₂ flow of about 10,000 sccm or more and an NH₃ flow of about 1,000 sccm or less.

30

TI-35995

26. The method of claim 25, wherein depositing the low silicon-hydrogen SiN material comprises performing the plasma enhanced chemical vapor deposition process with an N₂ flow of about 14,000 sccm or more.

5

27. The method of claim 25, wherein depositing the low silicon-hydrogen SiN material comprises performing the plasma enhanced chemical vapor deposition process with an NH₃ flow of about 750 sccm or less.

10 28. The method of claim 22, wherein the low silicon-hydrogen SiN layer is an etch stop layer in a poly-metal dielectric level.

29. The method of claim 22, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.04 or less.

15

30. The method of claim 22, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.03 or less.

31. A semiconductor device, comprising:
20 a ferroelectric capacitor formed in a capacitor level above a semiconductor body; and
a hydrogen barrier above the ferroelectric capacitor, the hydrogen barrier comprising a low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:

25
$$\text{Si-H absorbance} / (\text{N-H absorbance} \times 1.4).$$

32. The semiconductor device of claim 31, wherein the low silicon-hydrogen SiN layer is one of an etch stop layer in the capacitor level, an etch stop layer in a metalization level above the capacitor level, and an etch stop layer
30 in a protective oxide level above an uppermost metalization level.

TI-35995

33. The semiconductor device of claim 32, further comprising a second low silicon-hydrogen SiN layer above a transistor in the semiconductor device, the second low silicon-hydrogen SiN layer being below the capacitor level, the second low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:

$$\text{Si-H absorbance} / (\text{N-H absorbance} \times 1.4).$$

34. The semiconductor device of claim 33, wherein the second low silicon-hydrogen SiN layer is an etch stop layer in a poly-metal dielectric level.

35. The semiconductor device of claim 31, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.04 or less.

36. The semiconductor device of claim 31, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.03 or less.

37. A semiconductor device, comprising:
a ferroelectric capacitor formed in a capacitor level above a semiconductor body; and

a hydrogen barrier above a transistor and below the capacitor level in the semiconductor device, the hydrogen barrier comprising a low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:

$$\text{Si-H absorbance} / (\text{N-H absorbance} \times 1.4).$$

38. The semiconductor device of claim 37, further comprising a second low silicon-hydrogen SiN layer above the ferroelectric capacitor, the second low silicon-hydrogen SiN layer having an FTIR figure of merit value of about 0.05 or less, wherein the FTIR figure of merit is calculated as:

TI-35995

Si-H absorbance / (N-H absorbance x 1.4).

39. The semiconductor device of claim 37, wherein the low silicon-hydrogen SiN layer is an etch stop layer in a poly-metal dielectric level.

5

40. The semiconductor device of claim 37, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.04 or less.

41. The semiconductor device of claim 37, wherein the low silicon-hydrogen SiN layer has an FTIR figure of merit value of about 0.03 or less.

10